Troubleshooting Multiple-Bus Systems using FlexChannel® Input Channels

TECHNICAL BRIEF

Tektronix®

WHAT YOU WILL LEARN:

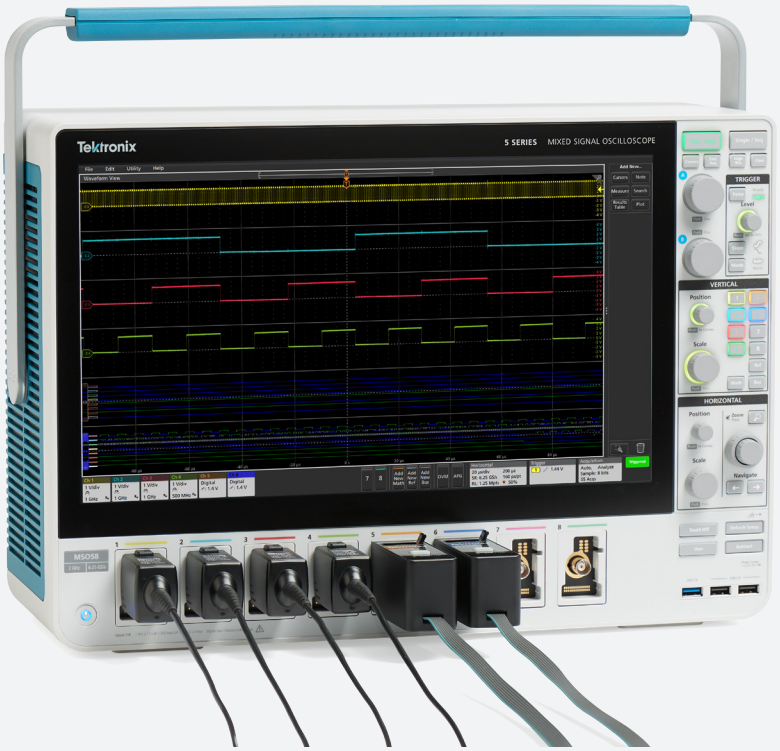
How to leverage the flexibility of a mixed signal oscilloscope equipped with FlexChannels® to debug and verify systems with a wide variety of parallel and serial bus configurations.

Introduction

Most embedded systems, even relatively simple ones, incorporate multiple bus structures. Being able to observe these systems requires debug and verification tools capable of displaying the activity of multiple buses, as well as sensor, actuator, display, and interface signals. Not only are you challenged with looking at multiple buses, but each bus may require a different approach to signaling, and therefore probing. Some can be observed using single-ended measurements, while others require differential measurements. In order to look at multiple buses, you may be able to take advantage of digital logic channels to greatly expand your channel count. This application note discusses the challenges embedded system designers face in evaluating multi-bus systems, and how to overcome them especially using FlexChannel input channels.

New FlexChannel input channels help to address the need to measure many different signals by enabling the use of the widest range of probes. Each FlexChannel can measure:

- 1 single-ended analog signal with a passive probe
- 8 digital logic signals with a TLP058 logic probe to access 8 digital channels.
- 1 differential voltage with a TekVPI® differential voltage probe
- 1 optically-isolated differential voltage with the IsoVu™ Isolated Measurement System
- 1 current with a TekVPI® current probe



8-FlexChannel MSO58 with analog and digital probes connected.

TLP058 logic probe for 5 Series MSO may be attached to any FlexChannel to provide access to 8 digital signals

The 5 Series MSO is the ultimate tool for debugging and verifying multi-bus systems. It starts with the large, 15.6-inch high-definition display, which offers twice the display area of a 10.4-inch display and the high-definition resolution to support many signals and buses.

The 5 Series MSO includes 4-, 6-, and 8-FlexChannel® models enabling them to acquire twice as many analog signals as most oscilloscopes. Each FlexChannel also provides 8 digital inputs which are accessed simply by connecting a TLP058 logic probe.

In addition to being able to change back and forth from analog to digital signal acquisition, the FlexChannel's distinctive architecture allows for very tight integration of analog and digital acquisition. Analog and digital signals use the same trigger circuitry and are sampled at the same time at the same rate, removing analog/digital timing uncertainty from the measurement process.

Considerations for High–Fidelity Bus Signal Capture

ACQUIRING SINGLE–ENDED BUS SIGNALS

Many common low- and mid-speed buses use single-ended signaling, representing digital signals with specific voltages relative to system ground. These analog signals are typically captured using the standard passive voltage probes included with an oscilloscope or with a digital probe on a mixed signal oscilloscope. FlexChannel inputs support both of these probe types. Here are some important considerations:

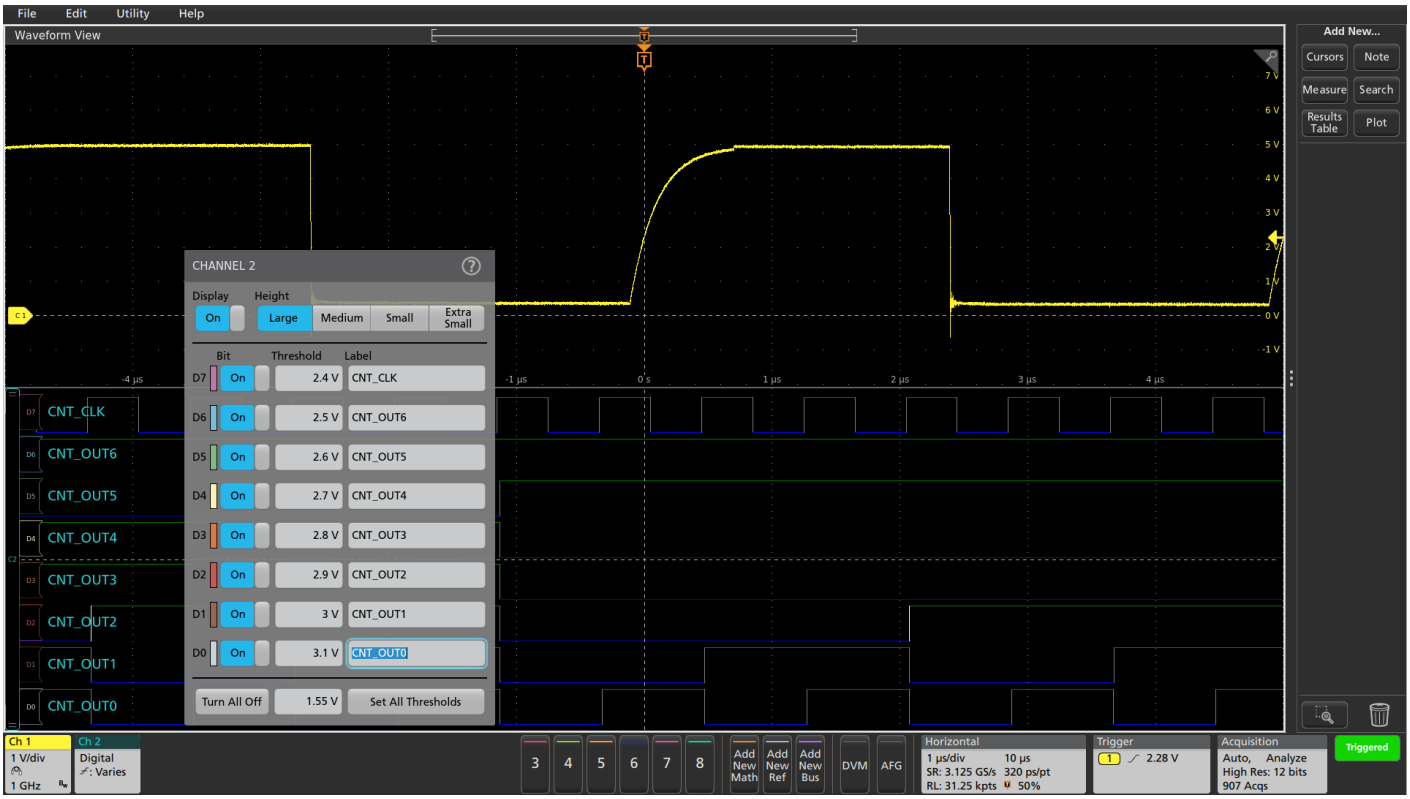
- Keep ground leads as short as possible. Successful acquisition of the analog signal begins with assuring that the reference voltages of each of the channels are connected to the oscilloscope through a low-inductance path.
- Assure that the rise-time of the measurement system is less than one fifth of the signal rise-time. The performance of the oscilloscope and probe must be adequate to faithfully represent the signal. A common guideline is to assure that the bandwidth of the measurement system is at least five times the bandwidth of the signal and that the sample rate is at least 3-5 times the signal bandwidth.
- For digital logic on MSOs, the system bandwidth of the oscilloscope and probe combination should be adequate to capture the signal, and the sample rate on the digital channel should be at least ten times the frequency of the signal. Performance is often specified in terms of bandwidth or, inversely, minimum detectable pulse width.
- Minimize probe loading effects on the signal by assuring the probe impedance is large compared to the signal's source impedance. For low-power circuits, this may be dominated by the probe's input resistance, while, for high-speed signals, this is dominated by probe input capacitance.

ACQUIRING DIFFERENTIAL BUS SIGNALS

To improve the noise immunity of bus signals and to improve the signal integrity of higher-speed buses, differential signaling is often used. Unlike single-ended signaling, differential signals are represented by the voltage difference between two signals. For some low-frequency applications, each side of the differential signal can be captured with a single-ended probe and the oscilloscope can calculate the mathematical difference. In practice, this technique is very susceptible to errors due to differences in probe gain, propagation delay, and compensation.

The most reliable way to capture a differential signal is to use an active differential probe, which uses a differential amplifier at the probe tip to sense the voltage difference.

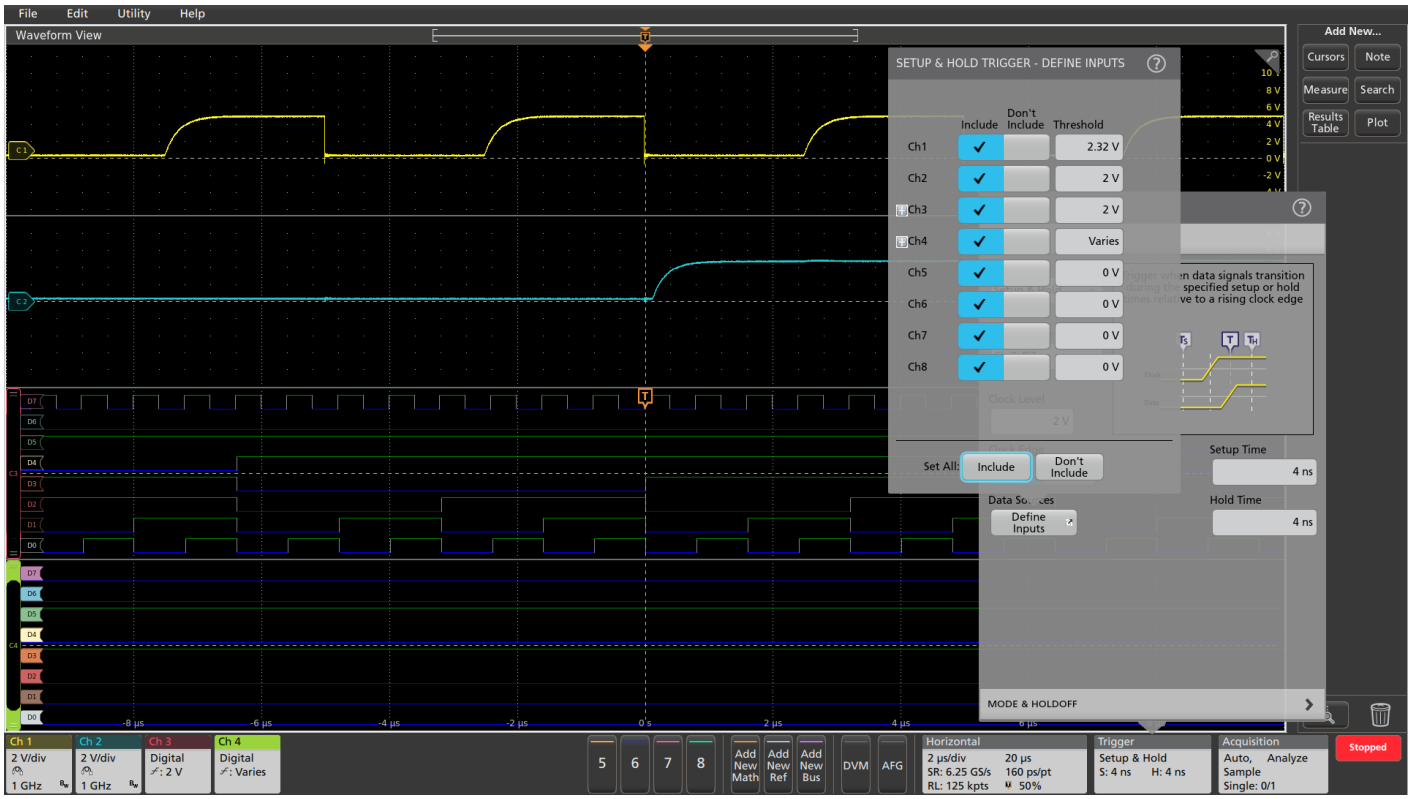
The performance considerations for single-ended probes, outlined above, still apply to digital probes. However, the ability of differential probes to ignore or reject common-mode signals must also be considered. The key specification for these probes is the Common Mode Rejection Ratio (CMRR) at the frequency of interest. Tektronix provides a range of differential probes at different performance level, including the optically-isolated IsoVu™ differential measurement systems for the most demanding measurement environments.



FOR ALL FORMS OF SIGNALING –– THRESHOLDS ARE KEY

No matter which technique is used to capture the signal, an analog representation of the bus signal is typically connected to the oscilloscope. Before the bus signal can be properly interpreted, the analog signal must be compared with a threshold value, above which the signal is typically interpreted as a high (“1”) and below which the signal is interpreted as a low (“0”). (In some cases, the analog voltages are compared to threshold values inside the digital logic probes.)

Many embedded designs are based on multiple logic families, requiring the use of a variety of digital thresholds. Oscilloscopes that allow per-channel thresholds enable maximum debug flexibility and acquisition fidelity.

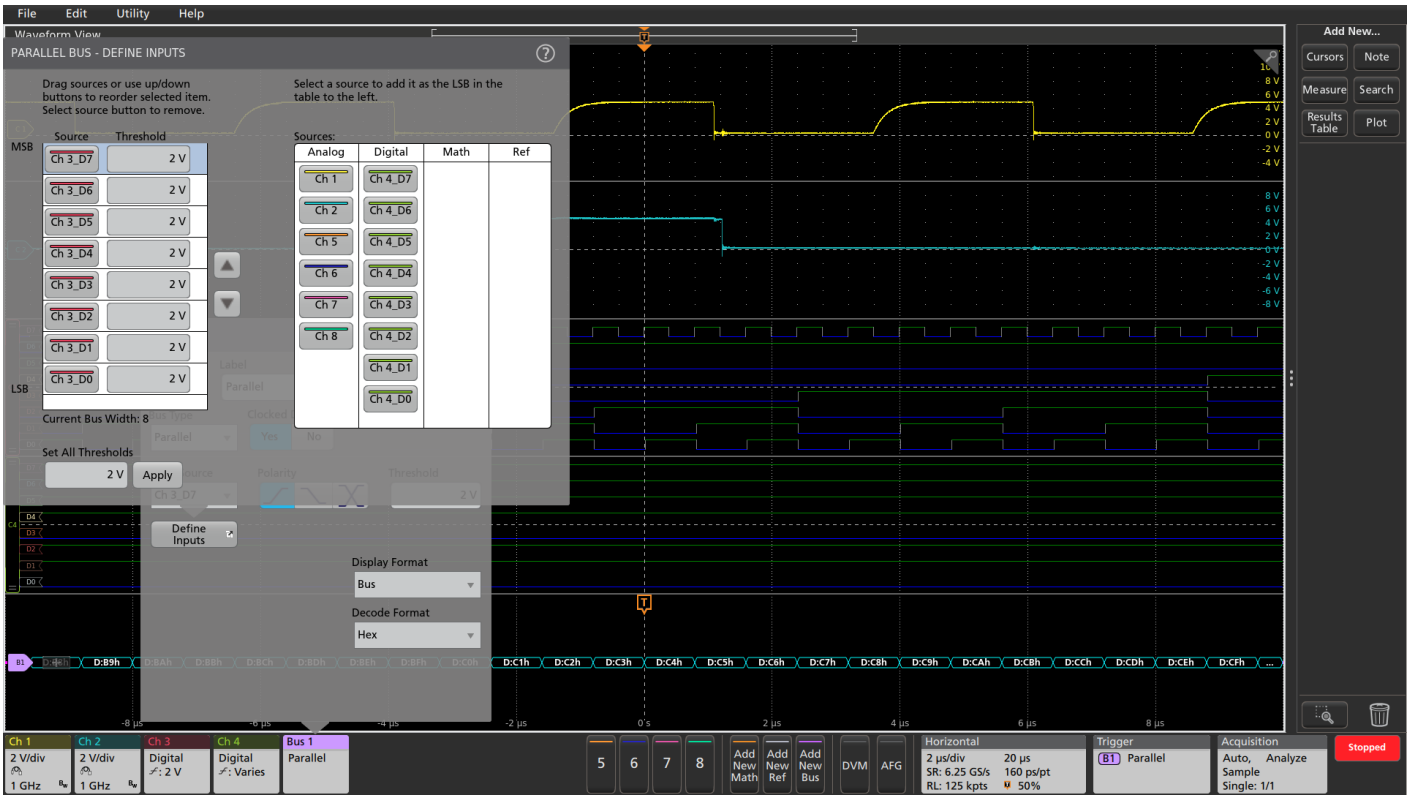


USING WAVEFORM TRIGGER MODES TO ISOLATE SIGNAL INTEGRITY ISSUES

When debugging signal integrity issues with parallel or serial buses, start with the standard trigger modes in an advanced oscilloscope to capture signals that violate the design specifications:

- Pulse Width triggering can be used to isolate glitches and minimum pulse width violations on clock and data lines.
- Timeout triggering can be used to isolate missing pulses, such as in a clock signal.
- Rise-time and Fall-time triggers can be used to isolate signal edges that are too fast or too slow for the design.
- Runt and Window triggering can be used to isolate digital signals that have improper amplitudes, either too low or too high.
- Multi-channel Setup & Hold triggering compares the timing of one or more data signals to the clock signals to detect violations of the component setup and hold times.

This example of standard digital debug triggering shows the bus setup and hold trigger configuration menu and display. Analog channels (channels 1, 2, and 5-8) and 16 digital inputs (channels 3 and 4) are available, and the oscilloscope is set to trigger on a timing violation.



Automated Bus Analysis

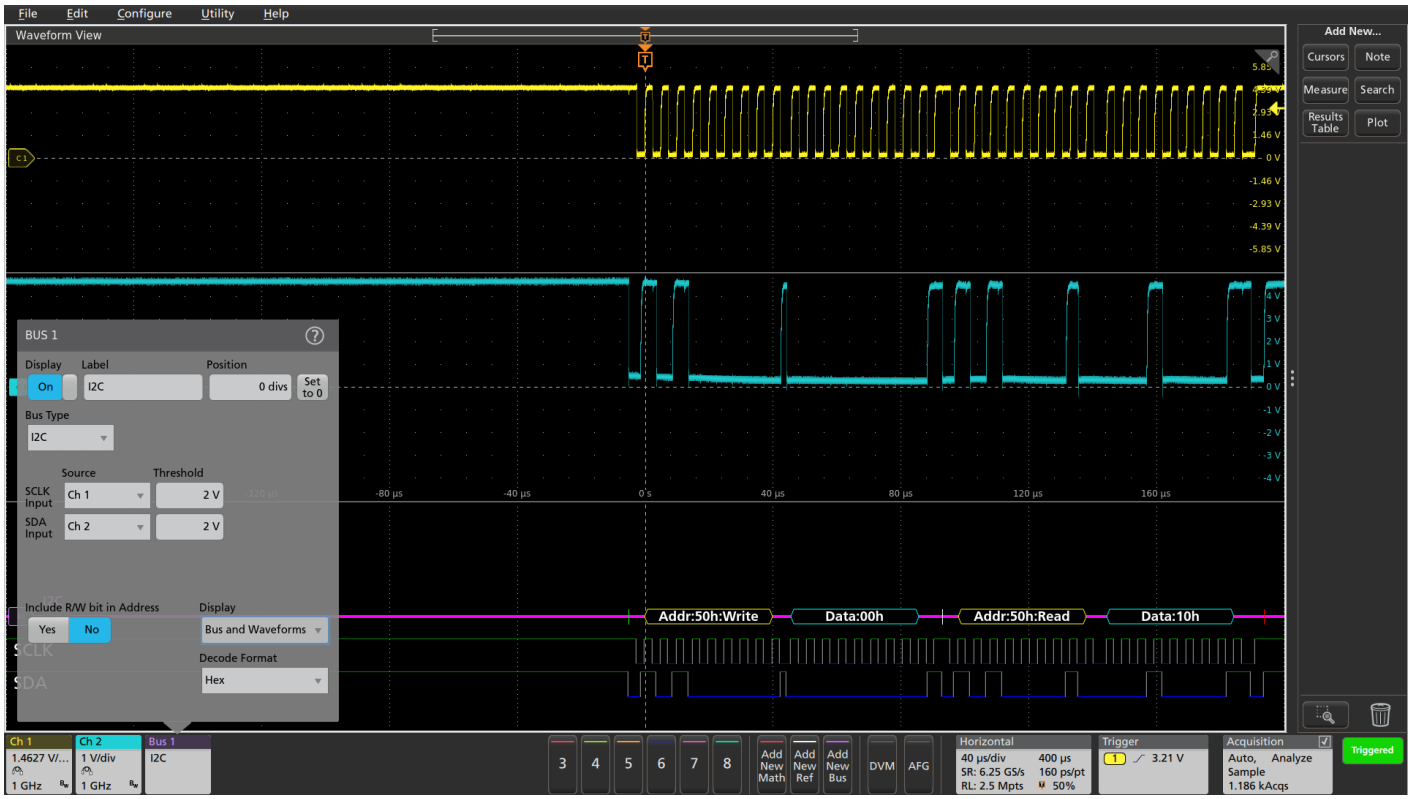
Once any signal integrity issues have been addressed, the next step is to verify that the broader system is working as expected.

DECODING BUS SIGNALS

With parallel bus architectures, each component of the bus has its own signal path. There may be address lines, data lines, a clock line, and various control signals. Address or data values sent over the bus are transferred at the same time over all the parallel lines. This makes it relatively easy to isolate an event of interest using the logic triggering found in most oscilloscopes. To decode the activity on a parallel bus, the logic state of each of the address, data, and control lines must be sampled at the appropriate time, usually coincident with the clock signal. The screen above shows a parallel bus setup configuration menu and display, showing that analog (channels 1 and 2) and 16 digital inputs (channels 3 and 4) are available, and triggering on a specific bus value.

On a serial bus, all this information is sent sequentially on one or a few conductors. This means that a single signal may include address, data, control, and clock information. As an example, consider the Inter-IC (I^2C) serial bus, where the clock is transmitted on one conductor and the data signal is transmitted on a second.

Armed with knowledge of the I^2C protocol, bus traffic can be manually decoded by capturing the signals, finding the start of the message (data going low while the clock is high), manually inspecting and writing down the data value on every rising edge of the clock, and then organizing the bits into the message structure. But this is a very time-consuming and error-prone process – not an efficient way to get a high-quality product to market.

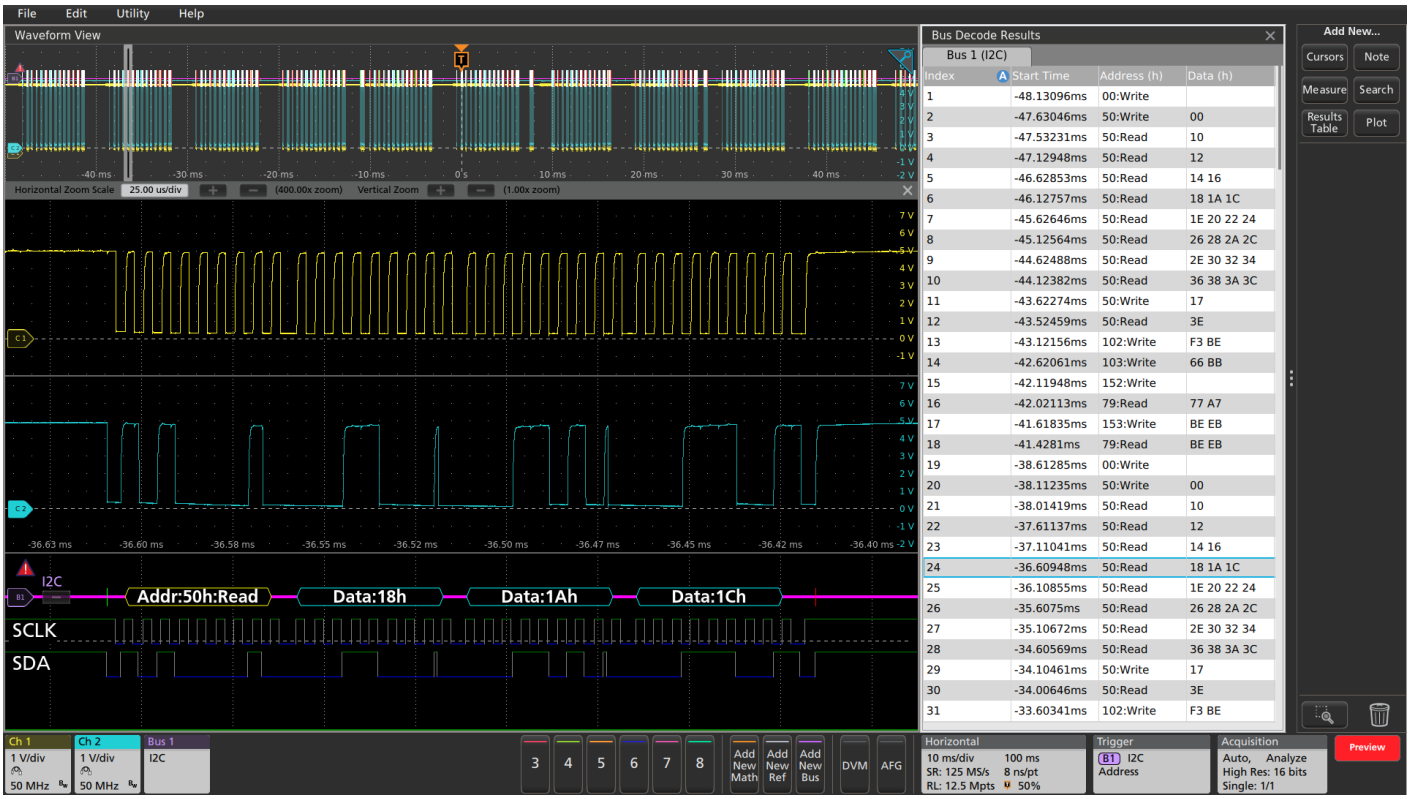


There is a better way. The example above shows an I²C serial bus setup for automated decoding and triggering. It shows the configuration menu, decode display incorporating analog input signals, and digital waveforms. The decoded bus traffic triggered on a bus write to address 50 hex.

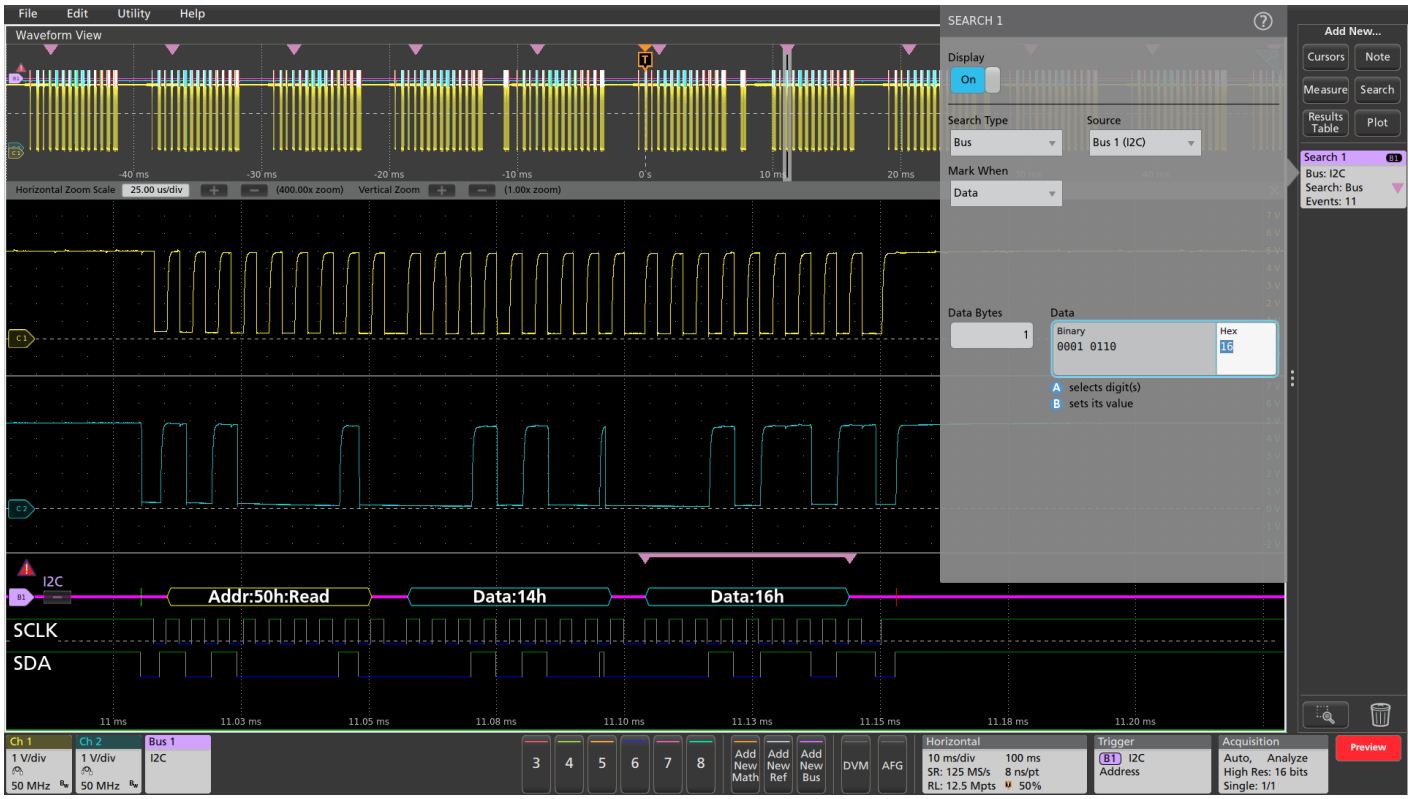
These sorts of optional bus analysis tools are available for some of the most common low- and mid-speed serial standards used in embedded system design. Support for parallel and serial bus standards vary depending on the oscilloscope model. Appendix A shows the bus support available on the 5 Series MSO. For bus support information on other oscilloscope series, please visit www.tektronix.com.

Notice the digital waveforms displayed below the decoded bus which show the results of comparing the analog input signals to the threshold values -- an intermediate step to decoding the serial bus. By visually comparing the analog and digital waveforms, this display can be used to verify that the threshold values are correctly set.

By visualizing key signals in the design before and after the trigger point, you can understand the causes and effects to debug problems and verify the system is operating as designed. For example, you can quickly find out that a system error occurs shortly after each bus write to a specific device.



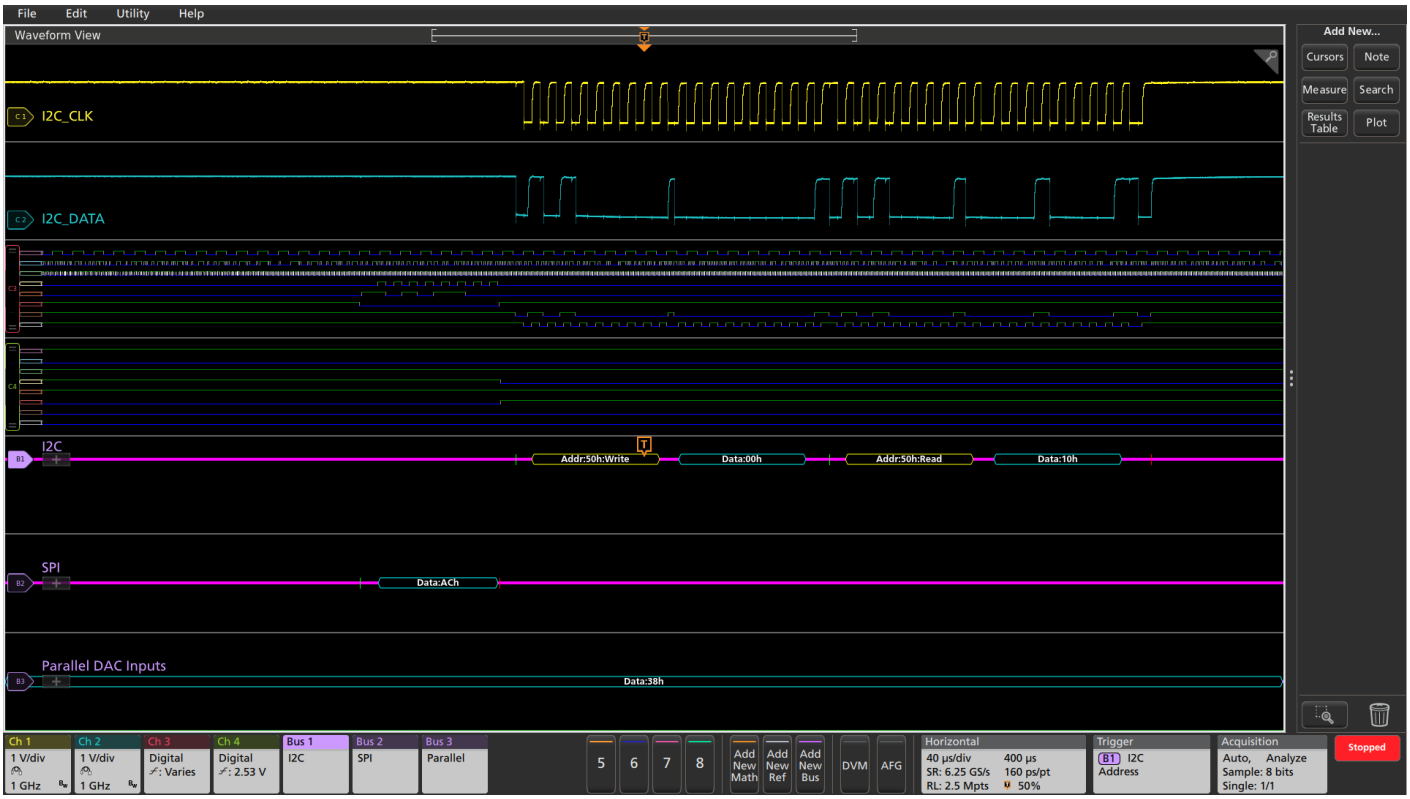
The time-correlated waveform and bus decode display is a familiar and useful format for many hardware engineers. For firmware engineers, however, the Results Table format may be more useful. This time-stamped display of bus activity can be easily compared to the software listings, and provides easy calculation of the execution speed.



AUTOMATED SEARCHING FOR SPECIFIC BUS EVENTS

When the bus trigger is correctly set up, the oscilloscope will capture all of the input signals and one specified bus event will be positioned at the trigger point. But how many of the events occurred? You can manually scroll through the acquired data to find the events. But that is time-consuming and error-prone.

A more efficient and reliable method is to use the automated Wave Inspector® search. The setup is similar to the bus trigger setup, enabling the oscilloscope to automatically find and mark all of the occurrences of the bus events of interest. In this example, the search is set up to look for Data value 16 hex on the I²C bus. Data byte 16 hex occurs 11 times in the acquired bus data, and each occurrence is indicated by a pink triangle at the top of the display. A detailed view of one of the matching serial data packets is shown with the pink bracket icon in the zoom window at the bottom of the display.



Multi–Bus Debug and Verification

Mixed signal oscilloscopes, outfitted with automatic bus decoding and triggering, are well-suited for debugging multi-bus systems. Once you are confident in the performance of one or more buses, plentiful digital channels may be used to provide insight into bus activity or to provide triggers. This allows you to reserve precious analog channels for gaining deeper visibility into signal quality.

This shows a multi-bus display on an 8-channel 5 Series MSO. It shows 3 buses in a synchronized view:

- I²C serial bus based on analog channels 1 and 2, using two single-ended passive probes
- SPI serial bus based on digital inputs on channel 3, using a TLP058 logic probe
- Parallel bus based on channel 4 digital inputs, using a TLP058 logic probe

By combining digital and analog channels the 5 Series MSO can support a number of buses, limited only by the combined number of channels.

Appendix A

BUS TRIGGERING, SEARCHING, AND DECODING AVAILABLE ON THE 5 SERIES MSO:

	TRIGGER / SEARCH ON:	BUS DECODE DISPLAYS:
Parallel (standard)	Data value (binary / hex)	Data value
I²C (option 5-SREMBD)	Start, Repeated Start, Stop, Missing Ack, Address (7 or 10 bit), Data (1-5 bytes), Address and Data	Start, Address, Data, Missing Ack, Stop
SPI (option 5-SREMBD)	SS Active (3-wire SPI), Start of Frame (2-wire SPI), Data (1-16 bytes)	Start, Data, Stop
RS-232 / RS-422 / RS-485 / UART (option 5-SRCOMP)	Start, End of Packet, Data (1 - 10 bytes), Parity Error	Start, Data, Parity, Parity Error
CAN (option 5-SRAUTO)	Start of Frame, Type of Frame (Data, Remote, Error, Overload), Identifier (Standard or Extended), Data (1-8 bytes), Identifier and Data, EOF, Missing Ack, Bit Stuff Error	Start of Frame, Identifier, Data Length Control, Data, CRC, End of Frame, Errors
CAN FD (option 5-SRAUTO)	Start of Frame, Type of Frame (Data, Remote, Error, Overload), FD Bits (FD Bit Rate Switch Bit, FD Error Status Indicator Bit), Identifier (Standard or Extended), Data (1-8 bytes), Identifier and Data, EOF, Error (Missing Ack, Bit Stuff Error, FD Form Error, Any Error)	Start of Frame, Identifier, Data Length Control, Data, CRC, End of Frame, Errors
FlexRay (option 5-SRAUTO)	Start of Frame, Indicator Bits (Normal, Payload, Null, Sync, Startup), Cycle Count, Header Fields (Indicator Bits, Identifier, Payload Length, Header CRC, and Cycle Count), Identifier, Data, Identifier and Data, End Of Frame (Static, Dynamic), Error (Header CRC, Trailer CRC, NULL Frame in Static, NULL Frame in Dynamic, Sync Frame in Dynamic, Start Frame No Sync)	TTS, Start, Frame ID, Payload Length, Headers, Cycle Count, Data, CRC, DTS, CID, Stop
SENT (option 5-SRAUTOSEN)	Start of Packet, Fast Channel (Status/Communication, Data), Slow Channel (Message ID, Data), Pause Pulse (Number of Ticks), Error (Frame Length, CRC)	Sync, Fast Channel Status, Slow Channel Message ID, Data, CRC, Pause, Errors
USB 2.0 (option 5-SRUSB2)	Token packet, Data packet, Handshake packet, Special packet, Error	Start, PID, Data, CRC, Stop
10/100BASE-T Ethernet (option 5-SRENET)	Start Frame Delimiter, Source and Destination MAC Addresses, MAC Q-tag Control Information, MAC Length/Type, MAC Client Data (1-16 bytes), IPV4 Header, TCP Header, TCP/IPv4 Client Data (1-16 bytes), End of Packet, FCS (CRC) Error, Idle	Start of Frame, Preamble, Start of Frame, MAC Destination and Source Addresses, MAC Length/Type, Data, IPv4 Header, TCP Header, Frame Check Sequence/CRC, End of Packet, Error
I²S / LJ / RJ / TDM (option 5-SRAUDIO)	Word Select (I²S, LJ, RJ only), Frame Sync (TDM only), Data	Left Channel Data (I²S, LJ, RJ), Right Channel Data (I²S, LJ, RJ), Channel 1 – N Data (TDM)
ARINC429	Word Start, Label, Data, SSM, SDI, Label and Data, Word End, Error (Any Error, Parity Error, Word Error, Gap Error)	Word Start, Label, SDI Field bits, Data, SSM, Parity, Word End, Errors
MIL-STD-1553	Sync, Command Word, Status Word, Data (16 bits and Parity), Time (RT/IMG), Error (Parity Error, Sync Error, Manchester Error (trigger only), Non-Contiguous Data)	Sync, R/T bit, Word Count, Status Bits, Parity, Address, Data, Errors

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